In the Claims:

1. (Currently Amended) A RAM store having a shared sense amplifier (SA) [[SA]] structure, ~~comprising:~~

in which

sense amplifiers (SA) arranged in SA strips between two respective adjacent cell blocks ~~for use~~ are used by a plurality of bit line pairs from the adjacent cell blocks, and ~~wherein~~

the bit line pairs have respective charge equalization circuits individually associated with them ~~for the purpose of~~ and perform, upon applying a respective precharge control signal, charge equalization between the bit line halves of the respective bit line pairs in a precharge ~~phase; and~~ phase,

wherein

~~a shorting transistor that, when prompted by a control signal, connects the bit line halves of the bit line pairs that are in the precharge phase to oneanother, wherein the~~ a shorting transistor is arranged in or on a [[the]] respective sense amplifier (SA) jointly for all bit line ~~pairs.~~ pairs that can be connected to the respective sense amplifier, said shorting transistor being provided to connect, at the sense amplifier, the bit line halves of the bit line pairs that are in the precharge phase to one another when the shorting transistor is switched by a separate shorting control signal via a dedicated control line that is separate from the precharge control signal performing the charge equalization between the bitline halves of the respective bitline pairs.

2. (Canceled).

3. (Original) The RAM store as in claim 1, wherein a respective sense amplifier can be connected to a respective one of two bit line pairs from a left-hand and a right-hand adjacent cell block.

4. (Original) The RAM store as in claim 1, wherein a respective sense amplifier can be connected to a respective one of four bit lines pairs from a left-hand and a right-hand adjacent cell block.

5. (Original) The RAM store as in claim 1, wherein the separate shorting control signal supplied via the control line dedicated to the shorting transistors switches all of the shorting transistors in an SA strip.

6. (Original) A method for controlling a RAM store having the design of a shared SA structure, in which sense amplifiers arranged in SA strips between two respective adjacent cell blocks are respectively used by a plurality of bit line pairs from the adjacent cell blocks, comprising:

generating a connection control signal separately for each of the bit line pairs associated with the same sense amplifier for connecting the sense amplifier to the respective bit line pair actuated by the connection control signal; and

generating a precharge control signal for performing charge equalization between the bit line halves of the bit line pairs associated with the same sense amplifier in a precharge phase,

wherein the bit line halves of the bit line pairs associated with the same sense amplifier are shorted, when these bit lines pairs are in the precharge phase on account of the precharge

control signal supplied to them, by means of a shorting transistor arranged in or on each sense amplifier by supplying this shorting transistor with a dedicated shorting control signal.

7. (Original) The control method for a RAM store as in claim 6, wherein in the activation phase for a particular bit line pair, the latter's precharge control signal and the shorting control signal that is supplied to the shorting transistor are deactivated and only the connection control signal for this bit line pair is activated, and

wherein in the precharge phase that comes directly after this activation phase and in which none of the bit line pairs associated with the sense amplifier has been activated, the connection control signals for connecting the bit line halves of all bit line pairs associated with this sense amplifier are generated and the shorting transistor is supplied with the shorting control signal, and the bit line halves of all of these bit line pairs are supplied with a center level.

8. (Original) The control method for a RAM store as in claim 6, wherein for a redundancy design, in which a faulty bit line pair is replaced by a redundant bit line pair, both the precharge control signal for the intact bit line pair and the shorting control signal supplied to the shorting transistor are deactivated in the activation phase for an intact bit line pair among the bit line pairs associated with the same sense amplifier and only the connection control signal is activated, and, in the precharge phase which follows this activation phase and in which none of the bit line pairs associated with this sense amplifier has been activated, the connection control signal is activated exclusively for the previously activated, intact bit line pair up until the next activation command on the same bank, the shorting control signal for the shorting transistor is activated and the bit line halves of all bit line pairs associated with this sense amplifier have the same center level applied to them.

9. (Original) The control method for a RAM store as in claim 6,

wherein the connection control signal respectively connects one of two bit line pairs from the adjacent cell blocks to the respective sense amplifier in a bit line assessment phase.

10. (Original) The control method for a RAM store as in claim 6,

wherein the connection control signal respectively connects one of four bit line pairs from the adjacent cell blocks to the respective sense amplifier in a bit line assessment phase.

11. (New) A memory device comprising:

a first bitline pair including a first bitline half and a second bitline half;

a first equalization circuit coupled between the first bitline half and the second bitline half;

a second bitline pair including a first bitline half and a second bitline half;

a second equalization circuit coupled between the first bitline half and the second bitline half;

a sense amplifier having a first line coupled to the first bitline half of the first bitline pair and first bitline half of the second bitline pair and a first line coupled to the second bitline half of the first bitline pair and second bitline half of the second bitline pair;

a first isolation transistor pair coupled between the first bitline pair and the sense amplifier;

a second isolation transistor pair coupled between the second bitline pair and the sense amplifier; and

a shorting transistor coupled between the first line of the sense amplifier and the second

line of the sense amplifier, the shorting transistor located between the first isolation transistor pair and the second isolation transistor pair.

12. (New) The device of claim 11, further comprising:

a first plurality of dynamic random access memory cells coupled to the first bitline; and

a second plurality of dynamic random access memory cells coupled to the second bitline.

13. (New) The device of claim 12, wherein no shorting transistor is included between the first plurality of memory cells and the first isolation transistor pair and wherein no shorting transistor is included between the second plurality of memory cells and the second isolation transistor pair.

14. (New) The device of claim 11, further comprising a first control line coupled to the first equalization circuit and a second control line coupled to the shorting transistor, the second control line separate from the first control line.

15. (New) The device of claim 14, further comprising a third control line coupled to the third equalization circuit, the third control line separate from the first and the second control lines.

16. (New) The device of claim 14, wherein the sense amplifier comprises one sense amplifier in a strip of sense amplifiers, each sense amplifier in the strip including a shorting transistor that is coupled to the second control line.

17. (New) The device of claim 11, further comprising:

a third bitline pair including a first bitline half and a second bitline half;

a third isolation transistor pair coupled between the third bitline pair and the sense amplifier;

a fourth bitline pair including a first bitline half and a second bitline half; and

a fourth isolation transistor pair coupled between the fourth bitline pair and the sense amplifier.

18. (New) The device of claim 17, further comprising:

a third equalization circuit coupled between the first bitline half and the second bitline half of the third bitline pair; and

a fourth equalization circuit coupled between the first bitline half and the second bitline half of the fourth bitline pair.